AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. - 5. (Canceled)

6. (Currently Amended) A method of manufacturing a flash memory, comprising the steps of:

performing an ion implantation process for adjusting a threshold voltage on a semiconductor substrate;

sequentially forming a tunnel oxide film, a first polysilicon film and a pad ~~oxide~~ nitride film on the semiconductor substrate~~, sequentially~~;

etching the pad oxide film, the first polysilicon film, the tunnel oxide film and the semiconductor substrate to form a trench defining an active region and a device isolation region;

~~performing an annealing process for nitrifying a surface of the trench so as to form a nitride film for preventing~~ forming a nitride film on an entire surface of the trench by means of an annealing process to prevent the implanted ions for adjusting the threshold voltage from diffusing to the device isolation region;

forming a side wall oxide film ~~on the side wall of the trench while suppressing diffusion of the implanted ion for adjusting the threshold voltage to the device isolation region to the maximum extent~~ on a surface of the nitride film and a sidewall of the polysilicon film; and

forming a device isolation film by filling up inside the trench.

7. (Original) A method of claim 6, wherein the side wall oxide film is formed by a dry oxidation method at a temperature in the range of 800℃ to 950℃.

8. (Original) A method of claim 6, wherein the annealing process is performed under N_2O atmosphere at a temperature in the range of 800℃ to 900℃.

9. (Currently Amended) A method of claim 6, after the step of forming a device isolation film, further comprising the steps of[;]:

eliminating the pad nitride film;

forming a second polysilicon film for a floating gate on the structure where the pad nitride film is eliminated;

forming a dielectric film on the structure where the second polysilicon film is formed; and

forming a third polysilicon film for a control gate on the dielectric film.